SiFive/RISC-V Overview

Multi Core High performance computing

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SiFive Japan K.K.

Nov 16th, 2023
SiFive is the RISC-V founder & brand standard
Leading the commercialization effort since 2010
World’s largest technology work with SiFive to adopt RISC-V
Largest team & investment
Recognized as the Most Respected Private Semiconductor Company
2018, 2019, 2020, 2022

Founded by the inventors of RISC-V
Disruptive **Technology**

<table>
<thead>
<tr>
<th>Barriers</th>
<th>Legacy ISA</th>
<th>RISC-V ISA</th>
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</thead>
<tbody>
<tr>
<td>Complexity</td>
<td>1500+ base instructions</td>
<td>47 base instructions</td>
</tr>
<tr>
<td></td>
<td>Incremental ISA</td>
<td>Modular ISA</td>
</tr>
<tr>
<td>Design freedom</td>
<td>$$$ – Limited</td>
<td>Free – Unlimited</td>
</tr>
<tr>
<td>License and Royalty fees</td>
<td>$$$</td>
<td>Free</td>
</tr>
<tr>
<td>Design ecosystem</td>
<td>Moderate</td>
<td>Growing rapidly. Numerous extensions, open and proprietary cores</td>
</tr>
<tr>
<td>Software ecosystem</td>
<td>Extensive</td>
<td>Growing rapidly</td>
</tr>
</tbody>
</table>
Unconstrained **Opportunity**

**RISC-V Business Model**

- Collaboration partners
- Development
- Supply chain
- Expanded markets
- Expanded geographies

**Barriers removed**
- Design risk
- Cost of entry
- Partner limitations
- Supply chain
RISC-V International

Industry innovation on RISC-V

- **Hardware** - RV64, multi-heart CPUs, vectors, bit manipulation, hypervisors, debug mode –
- **AI SoCs Application processors**
- **Software**
  - Linux
  - Drivers
  - AI Compilers

- **Hardware** - RV32, privilege modes, interrupts –
- **IoT SoCs Microcontrollers**
- **Software**
  - RTOS
  - Firmware

- **Hardware**
  - RV32 –
- **Proof of Concept SoCs**
  - Minion processors for power management, communications, ...

- **Software**
  - Bare metal software

- **Hardware ISA Definition Test Chips**
- **Tests**

|------------|-------------|-------------|-------------|------|

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The Rise of RISC-V

Over 80 billion RISC-V cores projected to ship by 2025

Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of 80 billion RISC-V cores by 2025.

SoCs shipping with RISC-V between 2020 and 2025 projects 114.9% CAGR.

Source: Semico Research

Over 3,800 RISC-V International members across 70 countries.
Rapid RISC-V growth led by industrial

Semico Research predicts the market for RISC-V CPU cores will grow at 114.9% CAGR from 2020-25. By 2025, RISC-V cores will capture over 14% of the overall CPU core business across all major end applications, targeting a broad range of performance levels.

 Nearly 80 billion RISC-V CPU cores by 2025

Source: Semico Research Corp, March 2021
RISC-V International now > more than 3,800 members
70 countries
Free, open, extensible ISA for all computing devices
350+ Design wins
100+ Customers
8 of 10 Top semiconductor companies work with us
600+ Employees
$2.5+B Valuation
RISC-V is Inevitable

The ecosystem of the Future is already being deployed

- The only major global compute platform on an open standard
- Used by all top semiconductor companies
- Supported by 3800+ members in RISC-V International
- Platform of choice in China & India
- Selected by US Govt
- Taught in all Top Universities
- Publicly embraced by Intel
- The strongest, most robust ecosystem is built on open standards with multiple participants
Legacy ‘efficiency processors’ are failing the industry

- Latest market requirements are not being met by current suppliers
- No innovation for the last 5 years
- SiFive’s latest innovation brings significant upgrade opportunities
- Vector compute brings performance boost and power efficiency
- SiFive Performance portfolio enables greater design flexibility
Broad Vertical Coverage

- **Enabling next-generation automotive**
  - EVs and ADAS are creating a unique catalyst for high-performance, low power compute

- **Infrastructure: Compute, AI, and China**
  - China server market has a strong preference for open standard RISC-V solutions
  - Heterogenous Compute and AI

- **Mission critical applications**
  - The most sensitive applications have adopted RISC-V due to its reliability, openness and durability
  - NASA adoption of RISC-V over Arm is a proof-point for large Aerospace, Defense and Industrial opportunities

- **Mobile**
  - Full Android support is coming! 
Google uses SiFive RISC-V cores in AI compute nodes

- At the AI Hardware Summit in Santa Clara, September 14th, Krste Asanovic, SiFive Co-Founder and Chief Architect, took to the stage with Cliff Young, Google TPU Architect and MLPerf Co-Founder, to reveal how the latest SiFive Intelligence™ X280 processor with the new SiFive Vector Coprocessor Interface Extension (VCIX) is being used as the AI Compute Host to provide flexible programming combined with the Google MXU (systolic matrix multiplier) accelerator in the datacenter.

Please find more detailed article in SiFive blog below.

https://www.sifive.com/blog/sifive-intelligence-x280-as-ai-compute-host-google
SiFive Product Portfolio

Four Product Families: Automotive, Essential, Intelligence, Performance

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<tr>
<th>Automotive</th>
<th>Intelligence</th>
<th>Performance</th>
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</thead>
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<td><strong>P870-A</strong></td>
<td><strong>X200-Series</strong></td>
<td><strong>P400-Series</strong></td>
</tr>
<tr>
<td>64-bit, High Perf Apps</td>
<td>AI processor for Edge and</td>
<td>&gt;8 SpecINT2k6/GHz</td>
</tr>
<tr>
<td>Processor</td>
<td>Data Center ML applications</td>
<td>3-wide OoO core</td>
</tr>
<tr>
<td>128b vector length</td>
<td>AI acceleration instructions</td>
<td>128b vector length</td>
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<tr>
<td>ASIL B, D and B/D</td>
<td>512b vector length</td>
<td>Hypervisor ext.</td>
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<tr>
<td>X280-A</td>
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<td>Vector crypto</td>
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<tr>
<td>AI acceleration instructions</td>
<td></td>
<td>IOMMU &amp; AIA</td>
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<tr>
<td>512b vector length</td>
<td></td>
<td>WorldGuard</td>
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<tr>
<td>ASIL B</td>
<td></td>
<td>RVA20</td>
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<tr>
<td>S7-A</td>
<td></td>
<td>P500-Series</td>
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<tr>
<td>64-bit, High Perf.</td>
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<tr>
<td>embedded ASIL D</td>
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<td>3-wide OoO core</td>
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<td>32-bit, balanced perf.</td>
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<td>IOMMU &amp; AIA</td>
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<td>WorldGuard</td>
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<tr>
<td>E2-Series</td>
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<td>RVA22</td>
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<tr>
<td>Smallest, most efficient</td>
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<td>P600-Series</td>
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<td>&gt;13 SpecINT2k6/GHz</td>
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<td>4-wide OoO core</td>
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<td>S2-Series</td>
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<td>Hypervisor ext.</td>
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<tr>
<td>64-bit, Area optimized</td>
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<td>Vector crypto</td>
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<td>WorldGuard</td>
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<tr>
<td>Balanced Perf.</td>
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<td>RVA22</td>
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<tr>
<td>ASIL B, D</td>
<td></td>
<td>P800-Series</td>
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<tr>
<td>ASIL D</td>
<td></td>
<td>&gt;18 SpecINT2k6/GHz</td>
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<td>6-wide OoO core</td>
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<tr>
<td>RVA22</td>
<td></td>
<td>RV64GCBV</td>
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**Essential**

<table>
<thead>
<tr>
<th><strong>U6-Series</strong></th>
<th><strong>U7-Series</strong></th>
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</thead>
<tbody>
<tr>
<td>64-bit, high</td>
<td>64-bit,</td>
</tr>
<tr>
<td>performance</td>
<td>superscalar</td>
</tr>
<tr>
<td></td>
<td>performance</td>
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<table>
<thead>
<tr>
<th><strong>S2-Series</strong></th>
<th><strong>S6-Series</strong></th>
<th><strong>S7-Series</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>64-bit, Area</td>
<td>64-bit, power</td>
<td>64-bit, high</td>
</tr>
<tr>
<td>optimized</td>
<td>efficiency</td>
<td>performance,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>embedded</td>
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<th><strong>E6-Series</strong></th>
<th><strong>E7-Series</strong></th>
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<td>Smallest,</td>
<td>Balanced Perf.</td>
<td>32-bit,</td>
</tr>
<tr>
<td>most efficient</td>
<td></td>
<td>optimized Perf.</td>
</tr>
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RISC-V is the Fastest Growing Software Ecosystem

- **Tools**
  - Ashley
  - Freedom Studio
  - Green Hills Software
  - Lauterbach Development Tools
  - SEGGER
  - WNDVR

- **Commercial Solutions**
  - wolfSSL
  - ProvenRun
  - Codeplay
  - Electrobit
  - SGS
  - Solid Sands
  - Wittenstein
  - RESILTECH

- **Android**
  - Android

- **Middleware, Libraries, Runtimes**
  - OpenMP
  - OpenSSL
  - NGINX
  - PHP
  - MySQL
  - SLEEF
  - PyTorch
  - OpenCV
  - TensorFlow

- **Non-Linux**
  - NetBSD
  - FreeRTOS
  - RTEMS
  - VxWorks
  - FreeBSD

- **Linux**
  - Yocto Project
  - Ubuntu
  - openSUSE
  - Debian

- **Foundational Software**
  - tianocore
  - AdaCore
  - GCC
  - LLVM
  - musl libc
  - KVM
  - LLVM
  - Virtual Open Systems
  - U-Boot

- **Execution Targets**
  - HiFive1
  - HiFive Unmatched
  - Microchip PolarFire
  - StarFive Vision Five
  - Dr. Who Inventor Kit
  - HiFive Pro P550
  - Xilinx VC138
  - Digilent Any 100T

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SiFive RISC-V Embedded Software Ecosystem

Open source solutions
Commercial solutions
SiFive RISC-V Linux Software Ecosystem

FreeBSD®

OpenMandriva

OpenWrt

Wireless Freedom
debian

defora

ubuntu

coreboot

gentoo linux™

OpenJ9

SUSE®

Linux

KernelCI

et

tianocore

NetBSD®

GCC
SiFive Automotive RISC-V Ecosystem

Compilers, RTOS, Virtualization, STL, Safety consultancy...
Android is Coming!

- Google has officially begun accepting RISC-V patches into Android Open Source Project (AOSP)
  - Keynote speech at the RISC-V summit by Google
  - AOSP - Android Open Source Project
    - Upstream open-source repository for Android
    - Enables community contributions to the codebase (like adding support for RISC-V)
- Google, and others, use AOSP as the basis for their commercial OS distributions
  - Android, FireOS, WearOS, etc… all base their OS on AOSP
- Note that AOSP support does not ensure Play Store support, but this is the first hurdle to clear
  - Native Java/Flutter apps will “just work”
  - High performance applications and libraries (game engines, etc..) will still need to be ported with Android SDK
Enhancing the SiFive Performance Portfolio
Extended family of area & power efficient processors
SiFive Performance™ Family

- Performance density leadership
- First with latest RISC-V features, standards, and technology
- High performance with optimized power efficiency
- SiFive momentum with NASA, Google, and Intel Horse Creek
## SiFive Product Portfolio

**Four Product Families: Automotive, Essential, Intelligence, Performance**

### Automotive
- **P870-A**
  - 64-bit, High Perf Apps Processor
  - 128b vector length
  - ASIL B, D and B/D

- **X280-A**
  - AI acceleration instructions 512b vector length
  - ASIL B

### Intelligence
- **P400-Series**
  - >8 SpecINT2k6/GHz
  - 3-wide OoO core
  - 128b vector length

- **P500-Series**
  - >8.6 SpecINT2k6/GHz
  - 3-wide OoO core
  - Hypervisor ext.
  - Vector crypto
  - IOMMU & AIA
  - WorldGuard
  - RVA20

- **X200-Series**
  - AI processor for Edge and Data Center ML applications
  - AI acceleration instructions 512b vector length

### Performance
- **P600-Series**
  - >13 SpecINT2k6/GHz
  - 4-wide OoO core
  - 128b vector length

- **P800-Series**
  - >18 SpecINT2k6/GHz
  - 6-wide OoO core

### Essential
- **U6-Series**
  - 64-bit, high performance

- **U7-Series**
  - 64-bit, superscalar performance

- **S2-Series**
  - 64-bit, Area optimized

- **S6-Series**
  - 64-bit, power efficiency

- **S7-Series**
  - 64-bit, high performance, embedded

- **E2-Series**
  - Smallest, most efficient

- **E6-Series**
  - Balanced Perf.

- **E7-Series**
  - 32-bit, optimized Perf.
SiFive Performance Family
2023 Product Lineup

P470
- >8 SpecINT2k6/GHz
- 3-wide OoO core
- 1x 128b VLEN RVV
- Vector crypto

P450
- >6.6 SpecINT2k6/GHz
- 3-wide OoO core

P650
- >11.5 SpecINT2k6/GHz
- 4-wide OoO core
- 1x 128b VLEN RVV
- Vector crypto
- Hypervisor extension
- IOMMU & AIA
- WorldGuard
- RVA22

P670
- >12.6 SpecINT2k6/GHz
- 4-wide OoO core
- 2x 128b VLEN RVV
- Vector crypto

Home Appliance
Wearable
Feature phone
Smartphone / Premium wearable
Network appliances

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SiFive Performance™ P470

**Boosted**
Performance

**Small**
Area

**Efficient**
Power

**Optimized**
Pipeline

**RISC-V**
Compliant

**Significant upgrade to legacy efficiency cores**

**Optimized area for power constrained applications**

**Highly-tuned for aggressively low power consumption**

**Out-of-Order pipeline enables optimal performance efficiency**

**Compliant with RVA22 profile, with support for Vector and Vector Crypto extensions**
SiFive Performance™ P670

**Highest**
Performance
Best-in-class performance

**Balanced**
PPA
Optimized performance within constrained area and power envelope

**Vector**
Extensions
Acceleration for media, crypto and data processing

**Feature**
Rich
Virtualization, IOMMU, AIA, Debug & Trace, Security

**RISC-V**
Compliant
Compliant with RVA22 profile, with support for Vector and Vector Crypto extensions
P470 Peak Single-Thread Performance

Cortex-A55: Performance 1.88GHz in 7nm, measured on Acer Spin 513 Chromebook with Qualcomm Snapdragon 7c. Area: 7nm TechInsights - Die photos show Cortex-A78 shortfall.

SiFive P470: Performance 2.97GHz in 7nm, 0.95V 32KB L1 I$ and D$, 2MB L2$. Area: measured in 7nm

Higher is better

Compute Density (SpecINT2k6/mm²)

4x compute density

Area with private caches (mm²)

Cortex-A55: ~0.43mm², P470: ~0.29mm²

Higher is better

Peak Single-Thread Performance (SpecINT2k6)

Cortex-A55: 20, P470: 16

Higher is better

4x compute density
Upgrade to the SiFive Performance Family

Performance density leadership

High performance with optimized power efficiency

First with latest RISC-V features, standards, and technology

The P400-Series and P600-Series are available to Lead Partners in Q4 2022
P870 High-Performance RISC-V Processor
RISC-V is based on standards

Standards Accelerate Software Adoption and Portability

Standards reduce cost
- Faster Adoption
- Compatibility across vendors

Layered standards enable customization
- RISC-V embraces customization without breaking compatibility

More than just ISA Standards
- RISC-V Standards extend beyond the Core ISA to system-level components
SiFive Performance family relentless innovation

- RVA20+
  - P550
- RVA22/RVA23
  - P650/P670
  - P450/P470
- RVA23
  - P870
  - P870-A

Customer In-Silicon Dates

- 2022
- 2023
- 2024

- More performance
- Higher core count
- Leading RISC-V feature deployment
- Automotive specific features

3rd generation OoO core
SiFive Provides Complete & Scalable Solutions

SiFive IP Complex

- CPU Clusters
- SiFive Cores
- Scalable Coherent Interconnect
  - Multi Cluster Interconnect
  - Shared L3 Cache
  - Up to 8 memory ports (CHI, AXI)
- Advanced Power Management
  - Advanced Interrupt Controller
  - SiFive Insight Debug & Trace
  - IOMMU
  - SiFive WorldGuard Security

Scalable High-Performance & High-Efficiency Cores: P870, P670, & P470 (with selected Mix+Match)

Shared Cluster L2 Cache

System IP to Enable Complete RISC-V SoC solutions
P870 µArch

- Instruction Cache 64KB
- NLP RAS Cond BP Ind BP
- 36-byte fetch
- Decode Rename Dispatch 6-wide
- Vector Sequencer
- Vector Disp Buffer
  - Iss Q
  - ADD MUL MAC
  - Crypt
  - Div
  - Perm
- Float Point Disp Buffer
  - Iss Q
  - ADD MUL MAC
  - Crypt
  - Div
  - Mask
- Integer Dispatch Buffer
  - Iss Q
  - ADD MUL MAC
  - DIV SQRT
  - ADD
  - MUL
  - MAC
  - ALU
  - BR
- Load/Store Dispatch Buffer
  - Issue Q
  - AGU
  - LD
  - LDST
- Data Cache 64KB
- Prefetchers
- Shared L3
- Cluster L2

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Cluster topology with shared L2 cache and distributed L3 cache

Legend:
- LSU - Load/Store Unit
- IEX - Integer Execution Unit
- FEX - Floating Point Execution Unit
- VEX - Vector Execution Unit
- IFU - Instruction Fetch Unit
- RDU - Rename/Dispatch Unit
P870 Consumer example platform
P870-A Functional safety features

- Advanced RAS architecture enabling error configuration, reporting, reaction and injection
- High integrity L2/L3 cache controllers and SECDED ECC
- Online diagnostic and STL
- SECDED ECC
- Core pairs in lockstep

Coherent Cluster bus

- L2$ slice 0
- L2$ slice 1

Core Cluster 0

- CPU Tile 0
- CPU Tile 1
- CPU Tile 2
- CPU Tile 3

Core Cluster 1

- CPU Tile 0
- CPU Tile 1
- CPU Tile 2
- CPU Tile 3

Cluster bus and crossbar with error detection code and error handling

L3 Cluster 0

- L3$ slice 0
- L3$ slice 1

Multi-Cluster Coherent Crossbar

Multi-Cluster Non-Coherent Crossbar

Memory Ports

System, Peripheral, Front ports

Debug

Interrupt

High integrity interrupt controller
SiFive Performance family relentless innovation

- RVA20+
  - P550

- RVA22/RVA23
  - P650/P670
  - P450/P470

- RVA23
  - P870
  - P870-A

- P870
  - More performance
  - Higher core count
  - Leading RISC-V feature deployment

- 3rd generation OoO core

- P870-A
  - Automotive specific features

- Napa
  - Customer In-Silicon Dates

Timeline:
- 2022
- 2023
- 2024
SiFive Core Designer enables configuration of SiFive RISC-V Core IP through an easy to use Web Portal.

- **Variants** are generated with a click of a button and are available from the Workspace.
- **Variants** contain:
  - RTL matching the configuration, including a testbench and other collateral needed to realize the design.
  - Documentation specific to the design.
  - Customized bare-metal BSP for easy integration into SiFive’s SDKs.
  - FPGA bitstreams for common FPGA development boards for easy software benchmarking of the RC.
Eclipse C/C++ Development Environment
- SiFive RISC-V Cross Compiler
- SiFive OpenOCD Debugger
- SEGGER J-LINK Debugger
- SiFive QEMU emulator
- SiFive Freedom E SDK software

RISC-V development tools
- GNU Newlib Toolchain
- OpenOCD
- QEMU
- SDK Utilities
- Trace Decoder
- XC3SPROG

Bare metal software development
- Example programs
- Industry standard benchmarks
- Board support
- Metal library

Embedded Linux software development
- Yocto / OpenEmbedded
- Board support
- Bootloaders
- Device tree binary
- Linux kernel images
- Disk images
Build and Run the Software

- File - Import - DevKit
  Examples - Browse

- Select the zip that matches your core

- Select the desired examples and click Finish

- Control-B will build the entire workspace

- Run - Debug - OpenOCD starts a JTAG Debug Session and Loads the program
Contact us

We’d love to hear from you!
Get In Touch

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Thank you

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